IN THE CLAIMS

1-12. (Canceled)

13. (New) A MIS-semiconductor-device manufacturing method comprising the steps of:

forming a gate dielectric on a semiconductor substrate of a first conduction type;

forming a gate electrode on a top surface of said gate dielectric;

forming a first side-wall spacer on a side wall of said gate electrode;

forming a first impurity area having a second conduction type opposite to said first conduction type by introduction of impurities into said semiconductor substrate with said gate electrode and said first side-wall spacer as a mask;

forming a second side-wall spacer by placing on said first side-wall spacer;

forming a second impurity area having an impurity concentration higher than an impurity concentration of said first impurity area by introduction of impurities into said semiconductor substrate with said gate electrode, said first

side-wall spacer and said second side-wall spacer as a mask; and

carrying out a heat treatment so that one edge of said gate electrode overlaps on said first impurity area,

wherein said first side-wall spacer is made of a material having a relative dielectric constant greater than that of said second side-wall spacer.

14. (New) A MIS-semiconductor-device-manufacturing method according to claim 13, wherein said first side-wall spacer is made of a material selected from the group consisting of silicon nitride, silicon, aluminum oxide, tantalum oxide, titanium oxide, zirconium dioxide and hafnium oxide.

15. (New) A MIS-semiconductor-device-manufacturing method according to claim 13, wherein said first side-wall spacer is made of a thin film having a fixed thickness.

16. (New) A MIS-semiconductor-device-manufacturing method according to claim 13, further comprising the step of forming silicon-oxide film on the surface of said semiconductor substrate and the surface of said gate electrode before forming said first side-wall spacer.

17. (New) A MIS-semiconductor-device-manufacturing method according to claim 13, wherein said first side-wall spacer has a width in the range from 5 nm to 15 nm.

18. (New) A MIS-semiconductor-device manufacturing method comprising the steps of:

forming a gate dielectric on a semiconductor substrate of a first conduction type;

forming a gate electrode on a top surface of said gate dielectric;

forming a first side-wall spacer on a side wall of said gate electrode;

forming a second side-wall spacer by placing on said first side-wall spacer;

forming a first impurity area having a second conduction type opposite to said first conduction type by introduction of impurities into said semiconductor substrate with said gate electrode, said first side-wall spacer and said second side-wall spacer as a mask;

forming a third side-wall spacer by placing on said second side-wall spacer;

forming a second impurity area having an impurity concentration higher than an impurity concentration of said first impurity area by introduction of impurities into said semiconductor substrate with said gate electrode, said first side-wall spacer, said second side-wall spacer and said third side-wall spacer as a mask; and

carrying out a heat treatment so that one edge of said gate electrode overlaps on said first impurity area,

wherein said first side-wall spacer is made of a material having a relative dielectric constant greater than that of said second side-wall spacer and said third side-wall spacer.

19. (New) A MIS-semiconductor-device-manufacturing method according to claim 18, wherein said first side-wall spacer is made of a material selected from the group consisting of silicon nitride, silicon, aluminum oxide, tantalum oxide, titanium oxide, zirconium dioxide and hafnium oxide.

20. (New) A MIS-semiconductor-device-manufacturing method according to claim 18, wherein said first side-wall spacer is made of a thin film having a fixed thickness.

21. (New) A MIS-semiconductor-device-manufacturing method according to claim 18, wherein said second side-wall spacer is made of a thin film having a fixed thickness.

22. (New) A MIS-semiconductor-device-manufacturing method according to claim 18, wherein each of said first side-wall spacer and said second side-wall spacer is made of a thin film having a fixed thickness.

23. (New) A MIS-semiconductor-device-manufacturing method according to claim 18, further comprising the step of forming silicon-oxide film on the surface of said semiconductor substrate and the surface of said gate electrode before forming said first side-wall spacer.

24. (New) A MIS-semiconductor-device-manufacturing method according to claim 18, wherein said first side-wall spacer has a width in the range from 5 nm to 15 nm.